RedCat Weekly Report

03.04.2007

As we have mentioned in the previous weeks report, this week we tried to send data from the Pc to the XSA-3S1000 board. We have tried so hard and saw the clearest view of how to send data to the XSA board and write the data to the RAM. We have started to design of a software which will help us to simulate sending data to the RAM that is to be done with the PIC in the forthcoming days of the project. This software will do the following and it will be very basic and understandable in order to have it implementable with the PIC. Basically, six of the parallel port data pins are used: one for a clock, one for a reset, and four for download data. The beginning 24-bit address for the downloaded data is broken into 4-bit pieces and downloaded to the FPGA on the rising edge of the clock. Then each 16-bit data word is broken into 4-bit pieces and downloaded into the SDRAM on the rising clock edge. After a word is stored in the SDRAM, the address is incremented and another 16-bit data word is downloaded.

So all our PIC has to do is receive the beginning address and the data words over a serial line and break these into 4-bit pieces that are sent through the parallel port interface of the XSA Board.

Here are the parallel port data pins that are used:

- D0 - reset for the downloading state machine in the FPGA
- D1 - clock for the downloading state machine in the FPGA
- D2 - D5 - 4-bit data bus

The pin assignments of the PIC will be as followed:

- PORTB,0 will be the reset pin as mentioned above.
- PORTB,1 will be the clock as mentioned above.
- PORTB,(2:5) will be used as data word that will send address and data information
- PORTB,(6:7) will be used for the configuration data acknowledge which we plan to use in the near future.

  These pins are all used in order to send data from the PIC.And of course, some acknowledge messages will be received from the XSA board in order to understand the state of the XSA board.These pins will be:
- PORTC,(3:0) that are status messages that are sent from the FPGA.

  Let us try to explain how we will send the data or namely the .xes formatted image file.The file will be sent from the PC via bluetooth line by line and there will be protocol that the PIC can understand that the beginning and the end of lines are received.These corresponding lines that have information of address and data <ADDRESS(23:0)><DATA(15:0)> will be stored in the PICs memory.Then tha transmission of the lines will be processed as explained.After a line is transmitted to the FPGA successfully, PIC will request the next line to be transmitted.